

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)
CS03-048

Application Number

Applicant(s)
Yisuo Li

Filing Date

Group Art Unit

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
WLL		US 5,970,300		(Buynoski)			
WLL		US 6,566,204		(Wang, et al.)			
WLL		US 6,599,804		(Bulucea, et al.)			
WLL		US 4,728,617		Woo, et al			
WLL		US 5,729,045		Buynoski			

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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jan 30,2004

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INITIAL

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Masahi Shima, "<100> Strained-SiGe- channel p-MOSFET with enhanced hole mobility and lower parasitic Resistance", Fujitsu Sci. Tech. J.,39,1, p. 78-83 (June 2003).

Oldiges, et al., " Molecular Dynamics Simulations of LATID implants into Silicon", found on Website <http://beam.helsinki.fi/~knordlun/pub/sispad97.pdf> ~ 3-1-2004 see <http://www.acclab.helsinki.fi/~knordlun/pub/>

Brand et al., Intel's 0.25 micron, 2.0V logic process technology, Intel.Technology Journal Q3,98, pp. 1-4.

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